Low Stress Packaging of a Micromachined Accelerometer

Gary Li and Ampere A. Tseng

***Abstract*—A packaging study of an acceleration microelectromechanical systems (MEMS) sensor is presented. The sensor consists of two silicon chips: a surface micromachined capacitive transducer (g-cell), which converts acceleration into signal of capacitance variation, and a microprocessor control unit (MCU) for signal conditioning. The two chips are die-bonded into a single piece of leadframe, connected via wire bonding, and finally molded with an epoxy compound. The primary goals of this paper are to provide insight and guidance for designing a package with low stress and low deformation. In particular, two die-bonding schemes: full die attach and four-dot die attach are presented in detail and their impact on performance of the transducer is discussed. Both the numerical simulation and testing data indicated that the four-dot die-attach process results in a significantly lower packaging stress to the transducer, and is appropriate for stress-sensitive MEMS devices.**

***Index Terms*—Die-attach, die-coat, MEMS packaging, micromachined accelerometer, sensor and actuator, stress and strain.**

I. INTRODUCTION

IN the past decade, tremendous progress has been achieved in designing and manufacturing prototypes of microelectromechanical systems (MEMS), and a new study foresees a potential MEMS market of $34.5 billion [6] by 2002. Among the numerous applications, automotive airbags have, by far, the largest market for micromachined accelerometers and rate gyroscopes [7]. The micromachined devices are batch processed, small in size, and thus result in a low cost relative to traditional mechanical sensing devices. They are also fragile and easily damaged, and therefore generally require two levels of packaging:

1) wafer level packaging, which is usually hermetic to provide damping control and to protect the MEMS devices from the subsequent dicing and testing;
2) conventional electronic packaging of die-bonding, wirebonding and molding to provide a housing for handling, mounting, and board level interconnection.

There are many factors, which must be carefully considered when designing a package for MEMS devices. First and foremost, the package must fulfill several basic functions:

1) to provide electrical connections and isolation;
2) to dissipate heat through thermal conduction;
3) to provide mechanical support and to isolate stress.

Manuscript received September 14, 2000; revised January 23, 2001. This work was supported by Motorola, Inc. and the U.S. National Science Foundation under Grants DMI-0002466 and DMI-9812984.

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Publisher Item Identifier S 1521-334X(01)04695-X.

Secondly, the packaging process must be stable, robust, and easily automated. Lastly, the design must take testability into account. An efficient means to test and trim an individual part and to isolate the source of defective components is essential in both reducing cost and subsequent quality improvement.

The cost of MEMS packaging is relatively high, and in some cases, can be as high as 80% of the total cost [3]. Reducing packaging costs is therefore a prime concern for both integrated devices, where the transducer and its signal conditioning unit are manufactured on the same silicon chip, and for two-chip (or multichip) designs. The two-chip approach, where the transducer and its signal processing microprocessor control unit (MCU) are fabricated separately and independently, becomes essential when some of the processings of the transducer are not compatible with processing of the MCU. The acceleration sensor described in this paper is a two-chip system.

II. MICRO-MACHINED ACCELEROMETER

The capacitive transducer considered in the present paper is designed in form of a differential capacitor pair made from three highly doped polysilicon layers using surface micromachining technology. The acceleration sensor is designed to be conveniently integrated into typical board configurations. As an example, Fig. 1 shows the two-chip accelerometer in an industry standard 16-pins dual-in line package (DIP). The detail of the micromachined transducer is shown in Fig. 2, a SEM micrograph obtained from [8]. The transducer is designed for 50 g full-scale acceleration having a supply voltage of 5 V with a 50-mV/g sensitivity. It operates in an open loop mode.

The three-layer transducer is structured having a bottom polysilicon layer adhering to the substrate, a top polysilicon layer anchored at various points in addition to the substrate, and a middle layer of polysilicon suspended by four tether beams. The middle layer, with the top and bottom layers respectively, forms two capacitors. When subjected to an inertial force, the middle layer is deflected. This motion in turn results in changes in capacitance for both capacitors, generating a differential output signal.

Mechanically, both the bottom and the top polysilicon layers have little motion relative to the substrate. The middle movable layer is an octagonal plate supported by four tethers, which are anchored to the substrate. The plate serves as the "proof mass" for the accelerometer, and contains 52 smaller holes spread over the plate and a larger hole in the center. The four tether suspension beams are made of polysilicon and silicon nitride layers.

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Fig. 1. Two-chip accelerometer in an industry standard 16-pins dual-in line package (DIP).

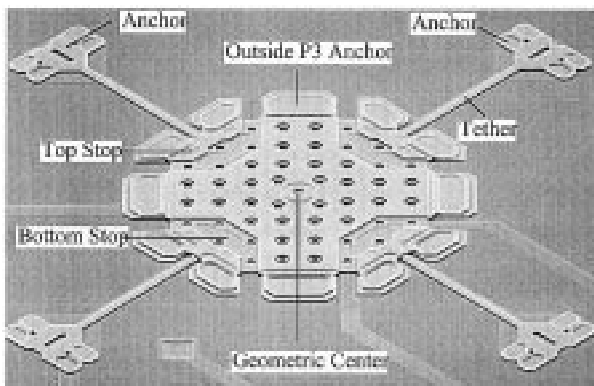


Fig. 2. SEM graph of a micromachined accelerometer (g-cell).

The combination of both nitride and polysilicon stresses is tensile along the tether, and therefore able to suspend the central plate. This transducer can be modeled as a mass-spring-dashpot oscillator.

III. Wafer-Level Packaging

Before the accelerometer can be put into a package of conventional leadframe-and-mold assembly, it must be sealed at the wafer level to protect the movable components from being damaged during the die sawing and subsequent molding. The wafer level package also provides the sensor with a controlled ambient to preserve the damping characteristics of the proof mass.

Motorola's wafer-level packaging is achieved through frit-glass bonding [2]. Sealing glass is first applied to the whole cap wafer in the form of a paste, which consists of a mixture of glass frit and an organic binder. The glass frit is deposited through a standard screen process. Following the screen process the capped wafer is allowed to dry, then fired at high temperature to burn off the organic binder and sinter the glass. To join the sensor wafer and the glass-coated cap wafer, the two are aligned and placed in close contact with one another. The assembly is then heated to a temperature exceeding the softening point of the glass and thermocompression-bonded to form a hermetic seal. Fig. 3 shows a schematic of a wafer-level

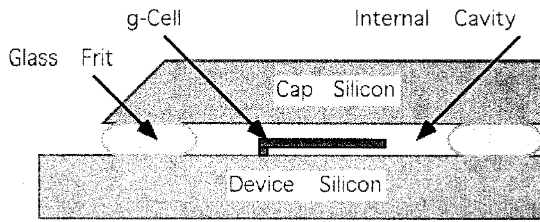


Fig. 3. Schematic of a wafer-level package of the micromachined accelerometer.

packaged accelerometer. The micromachined accelerometer is sealed inside the cavity formed by the device, cap wafers, and the glass frit.

IV. Packaging of the Capped Accelerometer

A. Basic Considerations for Sensor Packaging

There are three considerations when designing a package for sensors: electrical, thermal, and mechanical. The electrical and thermal considerations are common to all varieties of semiconductor devices, while the mechanical constraints can be unique in sensor packaging. The unique challenge of a sensor packaging is that in addition to providing a mounting foundation to a PC board, stresses induced by a mismatch in the thermal expansion coefficients of the materials used to fabricate the package and the external thermal loading of the package must be controlled and kept at a level low enough to avoid impact to the sensor performance. In general, different MEMS devices have different stress tolerance levels. Therefore, each MEMS package must be uniquely designed and evaluated to meet special requirements [4], [9]. Lastly, the packaging stress should also be controlled to be low enough such that it does not impact the performance of the control IC.

B. Assembly Sequence

After capping, the wafer-level packaged transducer and the signal conditioning circuitry are first mounted to a leadframe flag using epoxy as die-bonding material and using the standard die-bonding techniques. The two silicon chips are connected via standard wire bonding. A thin layer of silicone gel is then deposited over the transducer silicon die as passivation. In both the die-bonding and die-coating processes, curing is needed to ensure proper orientation after the viscous gel becomes solid. The final step involves the encapsulation of the two silicon chips in an epoxy mold compound, using conventional molding techniques, at a temperature of 165 °C. During the process of cooling (to room temperature), the die-coat shrinks more quickly than the mold compound, and a gap of approximately 25.4 μm (1 mil) is created. This air gap is used to shield stress transfer from the surrounding mold compound to fulfill the purpose of partial stress isolation.

A commercial finite element code, ANSYS, developed by ANSYS, Inc. of Canonsburg, PA, was selected for modeling the static behavior. Fig. 4 shows a partial view of a finite element model package model, where for clarity, only the mold compound under the leadframe flag is shown. The front face is actually the symmetric plane and the other half of the package is not shown. On the left is the control IC silicon, and on the right is the capped transducer silicon coated by silicone gel (commonly referred to as the die coat or dome coat). The tiny accelerometer (less than 1 mm in dimension) is hidden inside the g-cell cavity. The overall package footprint is 20×6.4 mm^2 (780×250 mil^2). In general, the size of a MEMS die may bear little relation to the package size, which is mainly dictated by compatibility requirements to the custom print circuit board.

C. Full Die-Attach Approach

The full die-attach approach refers to a die-bonding process in which the entire transducer silicon die is glued to the leadframe flag without void. It is achieved through dispensing a single drop of die-bond RTV into the flag and the silicon is squeezed into it in a controlled manner. This approach was recently developed by Motorola to appropriately control the amount die-coat underflow. In die bonding, unnecessary stresses can be generated if too much die-coat gel gets into under the silicon die, while not enough die-coat coverage can result in the silicon die to be unprotected. Details of this approach have been reported by [5] and [1].

The packaging induced stress or strain at room temperature can be calculated by the finite element model, using the ANSYS code. Due to the symmetric nature of the physical system, with proper boundary conditions, only half of the package needs to be modeled. It is understood that the attachment of electric leads into board could add some stresses and strains to the silicon transducer. However, based on a separate finite element calculation, the stress induced by the leads is smaller than 2% of the total stress and it has never been found that the induced stress is large enough to cause any problems or failures. Also, our focus is in evaluating the packaging impact to the transducer die. As a result, without complicating the modeling effort, the electric leads are not included in the FE model.

Assuming a stress free state of all components at the elevated temperature of 165 °C at which the molding takes place, both the package and the transducer die deformation at room temperature (25 °C) can be calculated. The resulting deformation contour is shown in Fig. 5 for the transducer silicon and its surrounding. It is clear that the maximum deformation occurs in the die-coat layer, whereas the transducer die suffers very little deformation and thus stress is indicated by a dark color in the shade spectrum. If the transducer silicon is isolated, a closer view of the deformation and stress near the region where the transducer is anchored can be obtained. By modifying the shade index and changing the amplifying factor, the deformed shape of the transducer silicon is shown in Fig. 6. Note that the maximum displacement in the silicon die is less than 0.305 μm (0.012 mil). Considering that the lateral dimension of the silicon die is 3.3 mm (130 mil), a displacement of 0.30 μm (0.012 mil) or less is indeed small, and the silicon die remains virtually flat under the packaging stress. After packaging, the accelerometer is trimmed for its sensitivity at room temperature. Therefore, the variation of silicon deformation away from room temperature, to either hot (90 °C) or cold (−40 °C), is critical and must be kept below the maximum level that the transducer can tolerate.

To help explain the simulation data, a Cartesian coordinate system is constructed and set on the top surface of the silicon

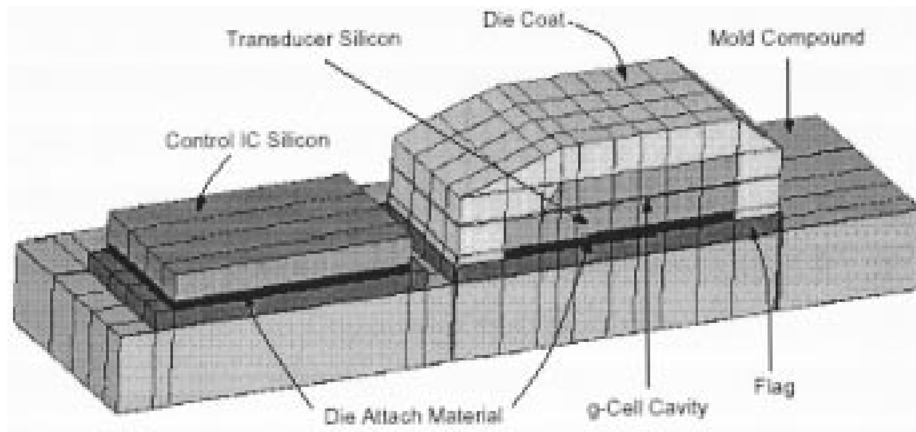


Fig. 4. Finite element model of a package of the microaccelerometer system. For illustration clarity, only half of the total system and only the partial molding compound (below the flag) are shown.

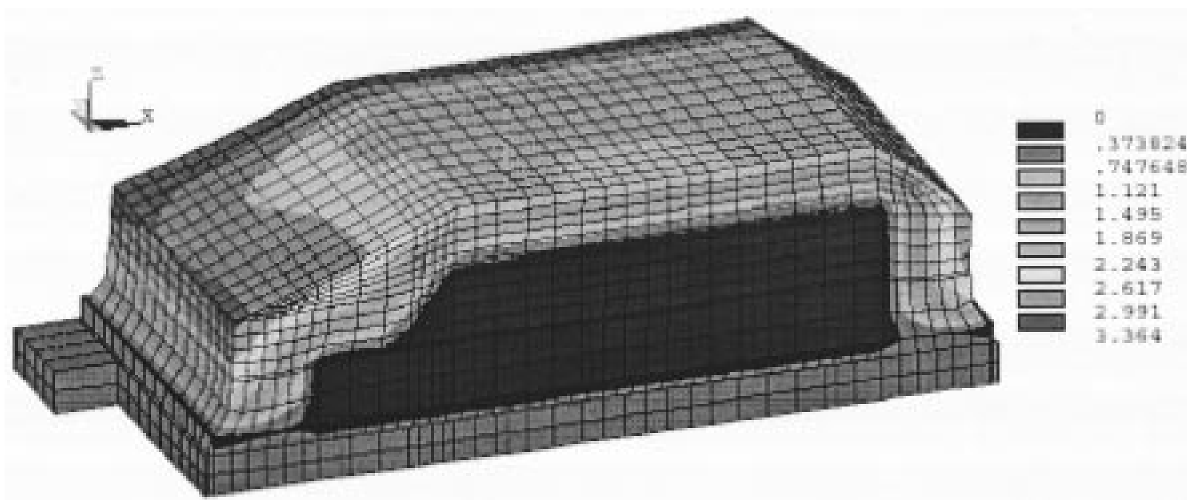


Fig. 5. Displacement contour for part of the total package at room temperature. Significant deformation occurred in the die coat while the silicon suffered very little deformation as illustrated by the dark color.

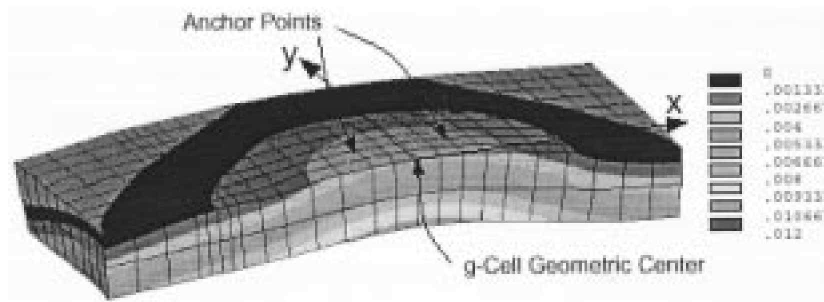


Fig. 6. Displacement contour of the device silicon (half is shown due to symmetry) at room temperature. Although very small, the silicon was bent by a force transmitted through the die bond.

die with the origin coinciding with the material point directly beneath the g-cell geometric center. The x-axis is along the longitudinal direction, and the y-axis is along the lateral direction and is perpendicular to x. Running the simulation for temperatures at −40, 25, and 90 °C, the resulting profiles of the vertical displacement are shown in Fig. 7; Fig. 7(a) depicts the displacement variations along the x-axis while Fig. 7(b) pictures the profiles cut along the y-axis. Clearly, the transducer silicon bends more at a cold (−40 °C) and less at a hot (90 °C) temperature. If the silicon state at room temperature is considered neutral, where trimming is performed, the bending due to a 65 °C temperature drop (to − 40°C) is about twice the bending caused by a 65 °C temperature rise (to 90 °C).

In order to evaluate the adverse impact on the performance characteristics of the transducer itself, in-plane displacements on the silicon surface at multiple locations are necessary. For simplicity and clarity, strain is calculated on the silicon surface rather than displacements. Once strain is known, displacement

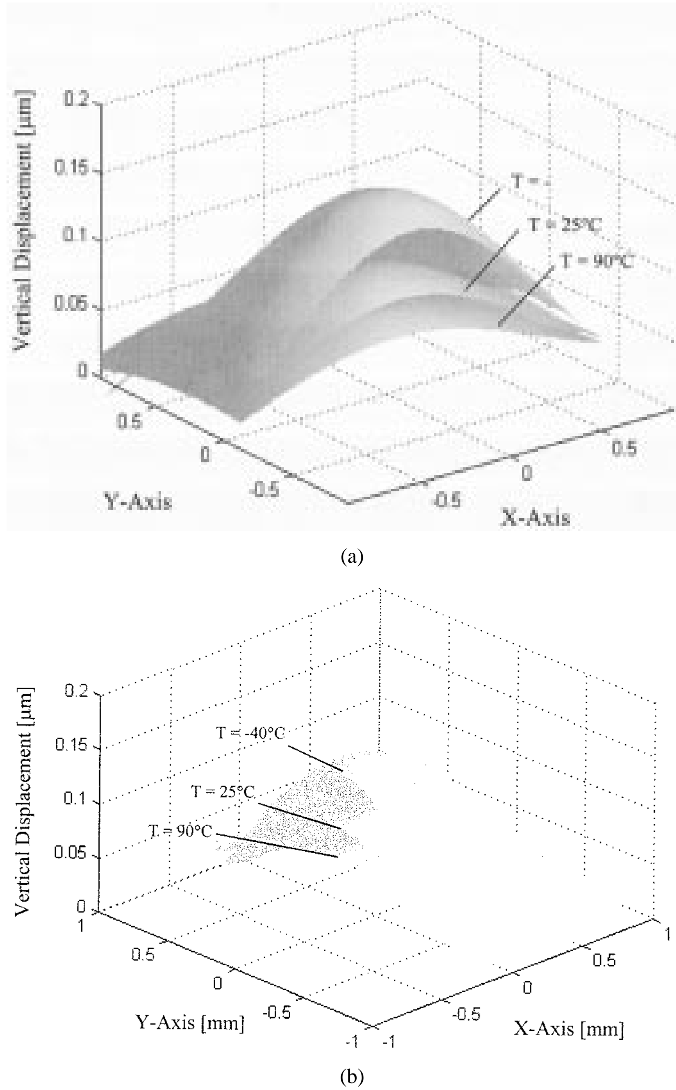


Fig. 7. Displacement profiles of device silicon bending at three temperatures (−40, 25, and 90 °C). An upward bending of the silicon is clear: (a) displacement profiles cut along the x-axis and (b) displacement profiles cut along the y-axis. An upward bending of the silicon is clear.

can be calculated in a straightforward manner. To evaluate the stress impact purely due to packaging, the silicon stress or strain induced by temperature variation must be subtracted from the total stress or strain. Consequently, we define the planar strain in the following manner:

$$\tilde{\varepsilon}_x = \varepsilon_x - \varepsilon_0 \tag{1a}$$

$$\tilde{\varepsilon}_y = \varepsilon_y - \varepsilon_0 \tag{1b}$$

where

- ε_0 denotes strain of the silicon alone (without the packaging effect);
- ε_x and ε_y represent the total strain on the upper silicon surface after packaging;
- $\tilde{\varepsilon}_x$ and $\tilde{\varepsilon}_y$ are used in analyzing the performance of the transducer itself.

We further introduce a single strain defined by

$$\varepsilon = \sqrt{\tilde{\varepsilon}_x^2 + \tilde{\varepsilon}_y^2} \tag{2}$$

which represents a combined strain on the upper silicon surface.

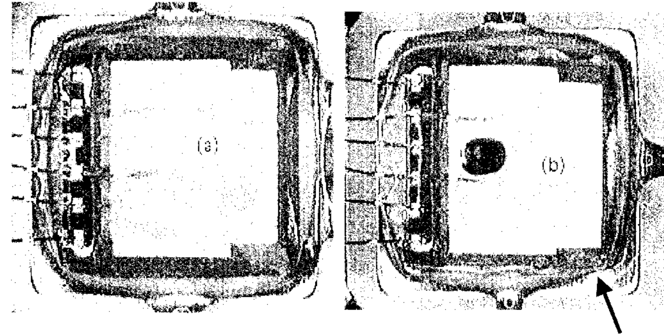
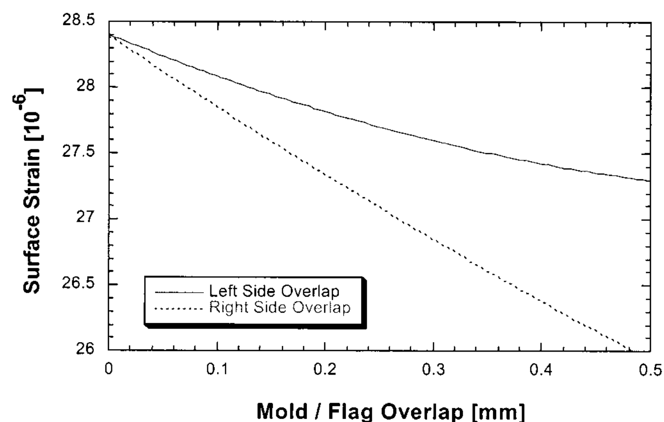


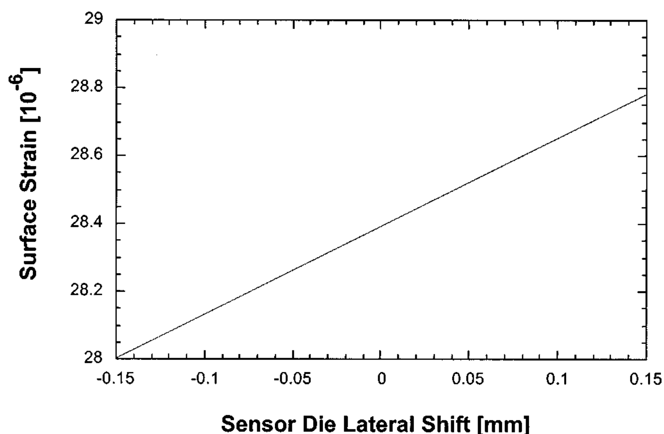
Fig. 8. Graphs of two partially packaged transducer dies: (a) nominal die-coat coverage and (b) less ideal die-coat coverage labeled by an arrow.

An issue that has received great attention in this packaging process is the control of die-coat thickness and uniformity. Production data show that the die-coat thickness often varies from die to die, and in extreme cases coat coverage can be entirely missed on the backside of the transducer silicon die causing direct contact between silicon and the mold compound. Fig. 8 shows the die-coat coverage; the white image in the central region is the transducer silicon die, while the dark color around the silicon die is the die-coat coverage. The die-coat compound is a sticky silicon gel dispensed to the top of the transducer silicon die (not the one for the control IC die) as shown in Fig. 4. The molding of the die-coat compound takes place at 160 °C. Since the coverage compound has a very high thermal coefficient, after cooling back to room temperature, the die-coat coverage can become nonuniform and be partially missed due to the much larger shrinkage of the die coat than the silicon die. Fig. 8(a) shows a nominal die-coat coverage while Fig. 8(b) depicts a die has less coat coverage on the lower right corner between the lead frame and the white-color silicon die as indicated by an arrow.

When in full coverage (nominal case), the die-coat ends at the edge of the leadframe flag and the flag is completely covered (except at two points where the leadframe flag under the transducer silicon joins the flag under the control IC). Thus, ideally, the mold compound in the nominal case is not in direct contact with the top surface of the transducer silicon. When the silicon die receives less coat coverage, for example on the right hand side as shown in Fig. 8(b), a portion of the flag is exposed and, after molding, the flag is effectively clamped by the mold compound. The thinner the die-coat, the greater the overlap between the flag and the mold. Numerical simulation was performed for a thinned coat coverage for both the left and right sides of the transducer silicon, and the result is shown in Fig. 9(a). The "Mold/Flag Overlap" of Fig. 9(a) refers to the overlap between the leadframe flag and mold compound. The vertical axis is strain as defined in (2). At zero overlap, which represents the nominal case where the gel coat covers the entire transducer die and the underneath flag footprint, a strain of 28.4 $\times\ 10^{-6}$ was obtained. At 508 μm (20 mil) overlap, where the gel coat was thinned to approximately 127 μm (5 mil), a lower strain was observed. The simulation data indicates that a thinner gel coat on the right side resulted in a smaller strain as compared to the strain from the similar thinned gel coat on the left-hand side. In a separate report [10], both analytical and numerical



(a)



(b)

Fig. 9. Variation of surface strain ε, at room temperature, as function o: (a) mold/flag overlap and (b) sensor die misplacement.

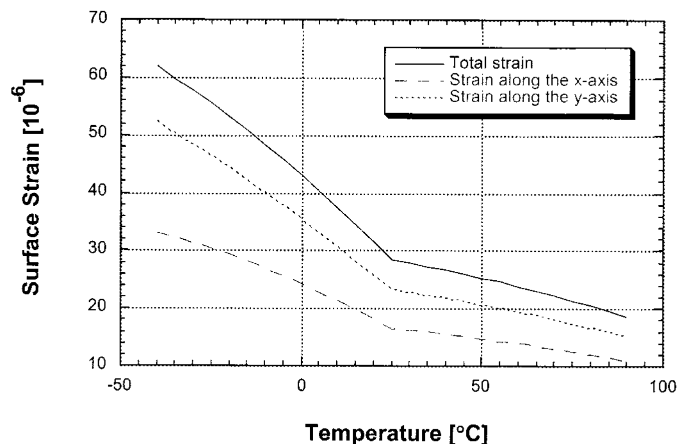


Fig. 10. Temperature dependence of the surface strain. The sudden change in slopes is caused by a change in the die-bond material property with temperature.

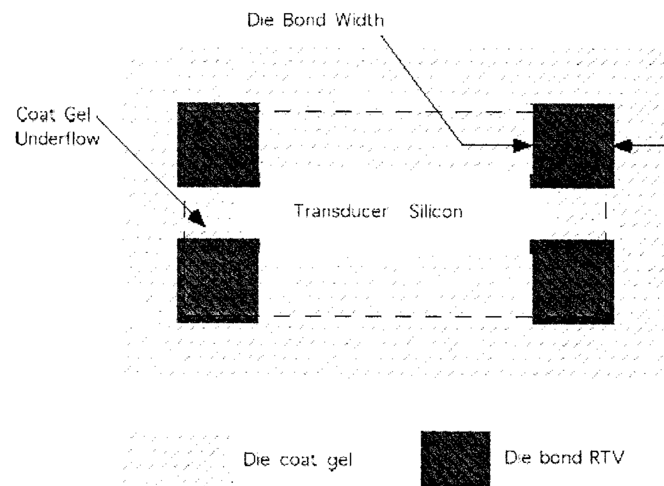


Fig. 11. Schematic of a four-dot die attaches. The size of die-bond drops can be controlled to ensure bonding reliability and a low packaging stress.

study showed that in order to maintain an air gap between the die-coat gel and the surrounding mold compound, a minimum of 127 μm (5 mil) gel coat must be dispensed surrounding the capped transducer die, which corresponds to a mold/flag overlap of 508 μm (20 mil).

Another consideration of this packaging process is the misplacement of the transducer silicon on the leadframe flag. It is of interest to calculate package stress variation when the die is slightly misplaced. For illustration purposes, a misplacement of up to 152.4 μm (6 mil), in both the positive and negative x directions, was assumed in the simulation, and the resulting strain ε is displayed in Fig. 9(b). Clearly, moving the transducer silicon to the left (toward the center of the leadframe flag) results in a lower stress.

Finally, since the sensitivity of the packaged micromachined transducer depends on the temperature induced stress or strain, it is of paramount importance to understand packaging stress variation relative to temperature such that a special design scheme can be incorporated into the signal control IC to compensate for the sensitivity gain or loss due to temperature variation. By varying the temperature from −40 to 90 °C, and calculating the strains on the silicon surface, the results are shown in Fig. 10. The dashed and dotted curves represent strain as defined in (1) in the x-and y-axis, respectively, and the solid curve is the combined strain as defined in (2). The packaging strain is high at the cold temperature and is monotonically decreasing as the temperature increases. The sudden change in slope is due to the nonlinear property (with temperature) of the die-bond material.

D. Four-Dot Die-Attach Approach

In addition to the full die attach process, an alternative die attach approach [1] was also researched and was adopted for some of the product lines. Realizing that the high stress level in the full die attach was primarily caused by silicon bending, it was hypothesized that removing the die-bond material in the central region directly beneath the sensing element should alleviate the bending and thus reduce packaging stress. By re-programming some of the die-bonding machines, the die-bond RTV could be dispensed at four points on the flag and the transducer silicon was subsequently squeezed to the flag with its four corners sitting on the four die-bond drops. Although the dispensed die-bond epoxy is usually round or elliptical, four small squares were utilized in the FEA modeling. If the stress and deformation in the central region of the silicon is the main concern, this approximation and simplification should result in little error according to St. Venant's Principle. Fig. 11 is a schematic showing

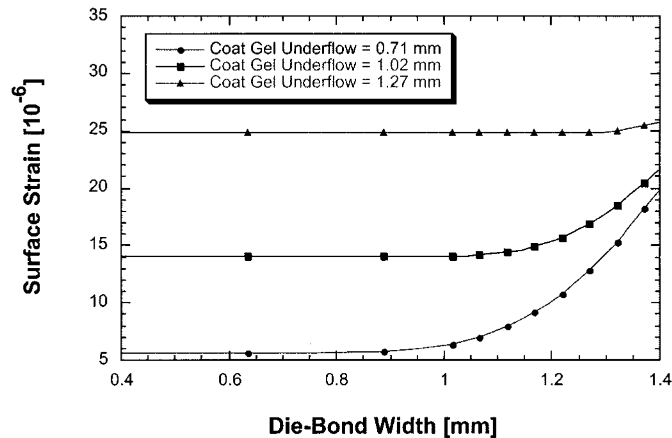


Fig. 12. Surface strain versus die-bond line width. A factor of five stress reduction can be achieved when the bond line width is controlled to be less than 889 μm (35 mil) and the coat gel underflow near 762 μm (30 mil).

four dots (four squares) of the die-attach epoxy at the four corners of the silicon. Also shown is the die-coat gel underflow (hatched area) which occurred during the coating and curing processes. The dashed rectangle represents the footprint of the transducer silicon.

There are three controllable parameters for the four-dot die-attach process:

1) die-bond width (size of the dispensed RTV);
2) die-bond thickness;
3) the die-coat gel underflow.

Assuming a nominal thickness of 76.2 μm (3 mil) RTV, the surface stress as a function of die-bond width and die-coat gel underflow is shown in Fig. 12. The result indicates that to achieve a lower stress in the central region of the transducer silicon, the bond width should be controlled to less than 1.02 mm (40 mil), and the gel underflow should be controlled to within 762 μm (30 mil).

V. Summary

The packaging processes for a micromachined two-chip accelerometer were described emphasizing the simulation aspect of the chip level packaging. The wafer level packaging involved frit-glass bonding to seal the mechanical transducer into a cavity, where the capping pressure was controlled for achieving optimal mechanical performance. The chip level packaging involved die-bonding both the transducer silicon and the control IC silicon to the leadframe flag, interconnecting both chips by wire-bonding, and finally encapsulating the total system by molding. Such a packaging process offers an alternative to monolithic fabrication and a solution to certain types of applications where the processing of the transducer is not compatible with the processing of its control IC.

The full die attach process resulted in a somewhat higher stress as compared to the four-dot process. The vast majority of this packaging induced stress was caused by silicon bending in addition to that caused by in plane stretching (or compression). The die-coat coverage also affects the packaging stress. It was found that, as long as the die-coat is sufficiently thick to guarantee the existence of an air gap between the gel coat and mold compound; a thinner die-coat resulted in a lower stress. In practice, this can be achieved through a leadframe with a larger flag footprint such that it allows sufficiently thick gel coat coverage without risking gel overflow and at the same time the flag can be imbedded into the mold compound after molding. To some degree the transducer silicon position on the flag also affects packaging stress. The simulation data shows that a lower stress may be obtained by moving the silicon die slightly to the left as indicated in Fig. 9(b).

Although the four-dot die attach process resulted in a lower packaging stress to the transducer, the precise control of the die-coat gel underflow may be difficult. Too much underflow would wipe out the benefit of the low stress from the four-dot die bonding process (see Fig. 12). Too little or no underflow may leave the possibility that the molding compound may compress under the silicon die and cause even more stress. After more than two years of experiments, the die bonding and die coating processes have become much more robust, and the yield loss due to packaging is significantly reduced. Currently, both the full die attach and the four-dot die attach processes are used in Motorola's packaging plants for different products.

Acknowledgment

The authors would like to thank P. L. Bergstrom, M. L. Ger, J. Foerstner, J. E. Schmiesing, F. A. Shemansky, D. Mahadevan, and M. K. Shah, for their constructive discussions and contributions.

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